2. (amended) The electronic phase-locked loop as claimed in claim 1, wherein that the digital phase-locked loop comprises a digital phase detector, a code converter, a PI filter, a drive circuit for the oscillator, the oscillator, which is designed as a digitally controllable crystal oscillator, and a counter, the lock detection being undertaken by the code converter.

3. (amended) The electronic phase-locked loop as claimed in claim 1, wherein by a configuration such that, in the event of transition of the digital phase-locked loop into a limit cycle with a phase error, called jitter, alternating between accuracy is canceled by the additional analog phase detector, the lock detection activating the analog phase detector via a line, said analog phase detector thereupon regulating both clock edges of the jitter in a continuously variable manner until said clock edges are synchronous with one another.

4. (amended) An integrated circuit having an electronic phase-locked loop of claim 1.

IN THE SPECIFICATION:

Please add the attached Abstract to the specification.

Respectfully submitted,

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